1. An integrated multiple transistor ESD protection structure on a semiconductor substrate, functionally connected to an integrated circuit input or output pin which will prevent electrostatic discharge damage to said integrated circuit comprising;

a first semiconductor layer having a first conductivity dopent type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopent concentration;

a third semiconductor layer having a second conductivity dopent type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopent type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer;

a plurality of third regions of said first semiconductor layer conductivity dopent type laterally spaced and interposed between said second regions;

2. The ESD protection structure of claim 1 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopent and form multiple collector elements of a bipolar transistor in which the bases are formed by said third conductivity layer and associated said plurality of second regions of p dopent, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopent.

3. The ESD protection structure of claim 1 whereby the protection structure is a bipolar npn transistor.

4. The ESD protection structure of claim 1 whereby said first collector regions have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

5. The ESD protection structure of claim 1 whereby said laterally spaced pluralities of third emitter regions are arranged in an alternating array within said third semiconductor base layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

6. The ESD protection structure of claim 1 whereby said third semiconductor emitter regions are electrically connected by a contact conductor element with N horizontal conductor stripe elements and further connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of said horizontal emitter stripes, and said base has horizontal contact regions interdigitated between said horizontal emitter stripes with the number of interdigitated horizontal base elements being equal to N+1.

7. The ESD protection structure of claim 1 whereby said third semiconductor emitter regions are electrically connected by a contact conductor element with N horizontal conductor stripe elements and further connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of said horizontal emitter stripes.

8. The ESD protection structure of claim 1 whereby one said p+ doped second semiconductor base horizontal contact region lies between said top horizontal collector contact and said multiple emitter contact regions, and a second said p+ doped semiconductor base horizontal contact region lies between the bottom horizontal collector contact and said multiple emitter contact regions enabling surface connections to said base regions

9. The ESD protection structure of claim 1 whereby said third semiconductor emitter regions are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous comb like manner by a vertical contact conductor element at one end of said horizontal emitter conductor stripes.

10. The ESD protection structure of claim 2 whereby said third semiconductor emitter regions are electrically connected by a contiguous contact conductor element with N horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of said horizontal emitter conductor stripes.

11. The ESD protection structure of claim 1 whereby said plurality of second semiconductor base region electrical contact conductors and said third semiconductor emitter region electrical contact conductors are ultimately connected together and to a second voltage source, typically ground.

12. An integrated multiple vertical npn transistor ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground which will prevent electrostatic discharge damage to said integrated circuit comprising;

a first semiconductor layer having a first conductivity dopent type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopent concentration;

a third semiconductor layer having a second conductivity dopent type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopent type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer.

a plurality of third regions of said first semiconductor layer conductivity dopent type laterally spaced and interposed between said second regions,

13. The ESD protection structure of claim 12 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopent and form multiple collector elements of a bipolar transistor in which the bases are formed by said third conductivity layer and associated said plurality of second regions of p dopent, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopent.

14. The ESD protection structure of claim 12 whereby said first collector regions have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

15. The ESD protection structure of claim 12 whereby said laterally spaced pluralities of third emitter regions are arranged in an alternating array within said third semiconductor base layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

16. The ESD protection structure of claim 12 whereby said third semiconductor emitter regions are electrically connected by a contact conductor element with N horizontal conductor stripe elements and further connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of said horizontal emitter stripes, and said base has horizontal contact regions interdigitated between said horizontal emitter stripes with the number of interdigitated horizontal base elements being equal to N+1.

17. The ESD protection structure of claim 12 whereby said plurality of second semiconductor base region electrical contact conductor elements and said third semiconductor emitter region electrical contact conductors are ultimately connected together and to a second voltage source, typically ground.

18. An integrated vertical npn multiple transistor ESD protection structure on a semiconductor substrate, functionally connected to an integrated circuit input or output pin which will prevent electrostatic discharge damage to said integrated circuit comprising ;

a first semiconductor layer having a first conductivity dopent type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopent concentration;

a third semiconductor layer having a second conductivity dopent type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopent type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer;

a plurality of third regions of said first semiconductor layer conductivity dopent type laterally spaced and interposed between said second regions;

19. The ESD protection structure of claim 18 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopent and form multiple collector elements of a bipolar transistor in which the bases are formed by said third conductivity layer and

associated said plurality of second regions of p dopent, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopent.

20. The ESD protection structure of claim 18 whereby said first collector regions have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

21. The ESD protection structure of claim 18 whereby said laterally spaced pluralities of third emitter regions are arranged in an alternating array within said third semiconductor base layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

22. The ESD protection structure of claim 18 whereby one said second semiconductor base horizontal contact region lies between said top horizontal collector contact and said multiple emitter contact regions, and a second said semiconductor base horizontal contact region lies between the bottom horizontal collector contact and said multiple emitter contact regions enabling surface connections to said base regions

23. The ESD protection structure of claim 18 whereby said third semiconductor emitter regions are electrically connected by a contact conductor element with N horizontal stripe elements and connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of said horizontal emitter conductor stripes.

24. The ESD protection structure of claim 18 whereby said plurality of second semiconductor base region electrical contact conductor elements and said third semiconductor emitter region electrical contact conductors are ultimately connected together and to a second voltage source, typically ground.

25. An integrated multiple vertical npn transistor ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground which will prevent electrostatic discharge damage to said integrated circuit comprising;

a first semiconductor layer having a first conductivity dopent type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopent concentration;

a third semiconductor layer having a second conductivity dopent type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopent type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer.

a plurality of third regions of said first semiconductor layer conductivity dopent type laterally spaced and interposed between said second regions,

26. The ESD protection structure of claim 25 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopent and form multiple collector elements of a bipolar transistor in which the bases are formed by said third conductivity layer and associated said plurality of second regions of p dopent, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopent.

27. The ESD protection structure of claim 25 whereby said laterally spaced pluralities of third emitter regions are arranged in an alternating array within said third semiconductor base layer,

with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

28. The ESD protection structure of claim 25 whereby said first collector regions have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

29. The ESD protection structure of claim 25 whereby said array comprises a said contact and said emitter contact region, and a said second semiconductor base horizontal contact region between the bottom horizontal collector contact and a "N" number of said n doped third semiconductor emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

30. The ESD protection structure of claim 25 whereby said third semiconductor emitter regions are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous comb like manner by a vertical contact conductor element at one end of said horizontal emitter conductor stripes.

31. The ESD protection structure of claim 25 whereby said plurality of second semiconductor base region electrical contact conductor elements and said third semiconductor emitter region electrical contact conductors are ultimately connected together and to a second voltage source, typically ground.

32. An integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground which will prevent electrostatic discharge damage to said integrated circuit comprising;

a first semiconductor layer having a first conductivity dopent type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopent concentration;

a third semiconductor layer having a second conductivity dopent type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopent type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer;

a plurality of third regions of said first semiconductor layer conductivity dopent type laterally spaced and interposed between said second regions;

33. The ESD protection structure of claim 32 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopent and form multiple collector elements of a bipolar transistor in which the bases are formed by said third conductivity layer and associated said plurality of second regions of p dopent, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopent.

34. The ESD protection structure of claim 32 whereby said laterally spaced pluralities of third emitter regions are arranged in an alternating array within said third semiconductor base layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

35. The ESD protection structure of claim 32 whereby said first collector regions have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin.

36. The ESD protection structure of claim 32 whereby said array comprises a said second semiconductor base horizontal contact region between the said top horizontal collector contact and said emitter contact region, and a said second semiconductor base horizontal contact region between the bottom horizontal collector contact and a "N" number of said n doped third semiconductor emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

37. The ESD protection structure of claim 32 whereby said third semiconductor emitter regions are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of said horizontal emitter conductor stripes.

38. The ESD protection structure of claim 32 whereby said plurality of second semiconductor base region electrical contact conductor elements and said third semiconductor emitter region electrical contact conductors are ultimately connected together and to a second voltage source, typically ground.

39. A Method for forming an integrated multiple transistor ESD protection device on a semiconductor substrate, functionally connected to an integrated circuit input or output pin which will prevent electrostatic discharge damage to said integrated circuit comprising;

forming a first semiconductor layer having a first conductivity dopent type;

forming a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopent concentration;

depositing a third semiconductor layer having a second conductivity dopent type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

forming a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

forming a plurality of second regions of said second conductivity dopent type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer;

forming a plurality of third regions of said first semiconductor layer conductivity dopent type laterally spaced and interposed between said second regions; and having a top element of conducting material making electrical contact external to said third regions;

40. The method according to claim 39 whereby said first semiconductor layer is formed of a heavily doped n+ material from either an arsenic or antimony ion implant process with an energy range of between about 25 and 30 KeV with a dosage of between about 10^{14} and 10^{15} a/cm^2 to produce a buried layer dopent concentration between 10^{18} and 10^{19} a/cm^3.

41. The method according to claim 39 whereby said semiconductor layer is a deposited n epitaxial layer doped with arsenic to produce a concentration of 10^{15} and 10^{16} a/cm^3.

42. The method according to claim 39 whereby said plurality of first regions are n+ semiconductor material created with either an arsenic or antimony ion implant with an energy range of between about 25 and 30 KeV with a dosage of between about10^{14} and 10^{15} a/cm^2 to

produce a dopent concentration between 10^{18} and 10^{19} a/cm^3 to form the collector contact regions.

43. The method according to claim 39 whereby said third semiconductor layer is a p layer bipolar base region created by an ion implant using boron as a dopent with an energy range of about 30 KeV with a dosage level of about 10^{12} a/cm^2 to produce a resultant concentration of about 10^{18} a/cm^3.

44. The method according to claim 39 whereby said second plurality of regions are p+ base contact regions formed from using boron in an ion implant with a dosage level of between 10^{13} and 10^{14} a/cm^2 to create a doping concentration of between 10^{18} and 10^{20} a/cm^3.

45. The method according to claim 39 whereby said third regions are n doped multiple emitter regions formed using a phosphorus ion implant with an energy range of about 30KeV and with a dosage level of between 10^{16} and 10^{17} a/cm^2 to create a doping concentration of 10^{19} and 10^{20} a/cm^3.

46.The method according to claim 39 whereby said collector electrical contacts are connected by either polysilicon or aluminum conductor elements to said integrated circuits input or output pins, and said base and emitter electrical contacts are electrically connected together by either polysilicon or aluminum conductor elements and connected to a second voltage source, typically ground.